JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

MCA I Semester
Computer Organization

Course Objectives:
The objectives of this course are to

- Conceptualize the basics of organizational and architectural issues of a digital computer.
- Learn the function of each element of a memory hierarchy.
- Study various data transfer techniques in digital computer.

Course Outcomes(COs): At the end of the course, student will be able to

- Understand the basic organization of computer and different instruction formats and addressing modes
- Analyze the concept of pipelining, segment registers and pin diagram of CPU.
- Understand and analyze various issues related to memory hierarchy
- Evaluate various modes of data transfer between CPU and I/O devices
- Examine various inter connection structures of multi processors

UNIT I:
Basic Structure of Computers: Functional unit, Basic Operational concepts, Bus structures, System Software, Performance- Processor clock, basic performance equation, pipelining and super scalar operations, clock rate, CISC,RISC, performance measurement, the history of computer development- generations.

UNIT II:
Instruction and Instruction Sequencing: Register Transfer Notation, Assembly Language Notation, Basic Instruction Types, Addressing Modes, Basic Input/output Operations, role of Stacks and Queues in computer programming equation. **Component of Instructions:** Logic Instructions, shift and Rotate Instructions.

UNIT III:
Type of Instructions: Arithmetic and Logic Instructions, Branch Instructions, **The Memory Systems:** Basic memory circuits, Memory System Consideration, **Read-Only Memory:** ROM, PROM, EPROM, EEPROM, Flash Memory, **Cache Memories:** Mapping Functions, interleaving, **Secondary Storage:** Magnetic Hard Disks, Optical Disks

UNIT IV:
Input/Output Organization: Accessing I/O Devices, Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access, **Buses:** Synchronous Bus, Asynchronous Bus, Interface Circuits, **Standard I/O Interface:** Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB)

UNIT V:
Processing Unit: Fundamental Concepts: Register Transfers, Performing an Arithmetic or Logic Operation, Fetching a Word from Memory, Execution of Complete Instruction, Hardwired Control, **Micro programmed Control:** Microinstructions, Micro program Sequencing, Wide Branch Addressing Microinstructions with next –Address Field

Text Books:

1. Computer Organization, 5th Edition, Carl Hamacher, Zvonks Vranesic, Safea Zaky, McGraw Hill
2. Computer Architecture and Organization,3rd Edition, John P. Hayes , McGraw Hill

Reference Books:

1. Computer Organization and Architecture, Sixth Edition, William Stallings, Pearson/PHI
2. Structured Computer Organization, 4th Edition, Andrew S. Tanenbaum, PHI/Pearson
3. Fundamentals or Computer Organization and Design, Sivaraama Dandamudi Springer Int. Edition